IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	Martin Czech	**GROUP:**	2815
SERIAL NO:	09/852,122	**EXAMINER:**	N. Drew Richards
FILED:	May 8, 2001		
FOR:	ELECTROSTATIC DISCHARGE PROTECTIVE STRUCTURE AND A METHOD FOR PRODUCING IT		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

PETITION UNDER 37 CFR §1.181

On August 16, 2006, the undersigned attorney submitted an Amendment, Petition and Fee for a three-month extension of time, and a check in the amount of $1,020.00 in response to the final Office Action dated February 21, 2006. A copy of the response filed is attached as Exhibit A. On August 29, 2006, an Advisory Action Before the Filing of an Appeal Brief was mailed to the undersigned. The Advisory Action states the Amendment filed will not be considered since the Amendment raises new issues and a Request for Continued Examination (RCE) was not filed. The undersigned submits the Advisory Action was issued in error since the last sentence at the bottom of the Petition and Fee for Extension of Time filed August 16, 2006 states "the Commissioner is authorized to charge any further extension and/or fee that is required to Deposit Order Account 50-3381." Therefore, the Commissioner clearly should have charged the required RCE fee to the

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I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date below, with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

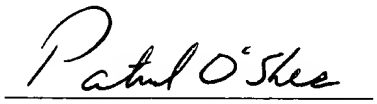
Sarah L. Henry

Date

deposit account in order for the Amendment to be considered. The undersigned respectfully requests the deposit account be charged the requisite RCE fee, and the Amendment be entered.

The Commissioner is authorized to charge any further extension and/or fee that is required to Deposit Order Account 50-3381. If a telephone interview could assist in the prosecution of this application, please call the undersigned attorney.

Respectfully submitted,



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8/16/2006

PAY TO THE ORDER OF Commissioner for Patents $ 1020.00

One Thousand and Twenty 00/100 DOLLARS

MEMO 3000-658 EOT

Patrick O'S Lee MP

[redacted]

O'SHEA, GETZ & KOSAKOWSKI, P.C. 2234

Date Received:

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AUG 18 2006
PATENT & TRADEMARK OFFICE

Ser/Pat/TM No. 09/852,122
File No. 6158
Inventor Name(s). M. Czech
Atty/Secretary PJO/lmw

August 16, 2006

Hon. Commissioner of Patents/Trademarks

Please acknowledge receipt of the attachments by stamping the date received in the space indicated and returning this card to the addressee. O'SHEA, GETZ & KOSAKOWSKI, P.C.

- ☐ Specification - # of pages
- ☐ Claims - # of pages
- ☐ Drawings - # of sheets
- ☒ Amendment
- ☐ Issue Fee/Publication Fee
- ☐ English translation document
- ☐ Assignment
- ☐ Marked up copy of specification/claims
- ☐ Clean copy of specification/claims
- ☐ Dec/POA
- ☐ Transmittal letter
- ☒ Check - $ 1,020.00
- ☐ IDS and PTO/SB/08A
- ☐ Copies of IDS citations
- ☐ Maintenance Fee
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	Martin Czech	**GROUP:**	2815
SERIAL NO:	09/852,122	**EXAMINER:**	N. Drew Richards
FILED:	May 8, 2001		

FOR: ELECTROSTATIC DISCHARGE PROTECTIVE STRUCTURE AND A METHOD FOR PRODUCING IT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

PETITION AND FEE FOR EXTENSION OF TIME

Pursuant to 37 CFR 1.136(a), petition is made for a THREE (3) month extension of time to file the attached Amendment, in response to the Office Action dated February 21, 2006.

A check in the amount of $1,020.00 is enclosed herewith.

The Commissioner is authorized to charge any further extension and/or fee that is required to Deposit Order Account 50-3381.

Respectfully submitted,

Patrick J. O'Shea
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I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on August 16, 2006 with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Kim M. Hume

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	Martin Czech	**GROUP:**	2815
SERIAL NO:	09/852,122	**EXAMINER:**	N. Drew Richards
FILED:	May 8, 2001		
FOR:	ELECTROSTATIC DISCHARGE PROTECTIVE STRUCTURE AND A METHOD FOR PRODUCING IT		

Assistant Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

AMENDMENT

This amendment is in response to the Official Action dated February 21, 2006. Please amend the application as follows:

IN THE CLAIMS:

Please amend claims 1-8 and 13-21 as follows:

1. (Currently Amended) An electrostatic discharge ~~(ESD)~~ protective structure that protects an integrated semiconductor circuit connected between a first potential bus with a first supply potential ~~(VCC)~~ and a second potential bus with a second supply potential ~~(VSS)~~, ~~said~~the electrostatic discharge protective structure comprising:

an electrostatic discharge diode having a first region doped with a first conduction type and a second region doped with a second conduction type~~, spaced apart from said first region~~;

~~said second region being doped with a second conduction type, wherein~~where ~~said~~the electrostatic discharge protective structure is located between the first and second potential busses and drains off an overvoltage pulse to one of the first and second potential busses, ~~wherein~~where ~~said~~the ~~laterally formed~~ electrostatic discharge diode includes a gate electrode located between ~~said~~the first region and ~~said~~the second region, ~~said~~the first region being separated from ~~said~~the second region by a distance that is equal to a width dimension of the gate electrode, and where ~~said~~the gate electrode and ~~said~~the second region are both directly connected to the second supply potential.

2. (Currently Amended) The electrostatic discharge protective structure of claim 1, ~~wherein~~where ~~said~~the protective structure includes a semiconductor body having a surface in which ~~said~~the first region and ~~said~~the second region are embedded, ~~wherein~~where ~~said~~the first region is connected via a first electrode to the first potential bus, and ~~said~~the second region is connected via a second electrode to the second potential bus.

3. (Currently Amended) The electrostatic discharge protective structure of claim 2,

~~wherein~~where ~~said~~the semiconductor body includes charge carriers of the second conduction type, and ~~said~~the gate electrode and ~~said~~the second electrode are connected to ~~said~~the second potential bus.

4. (Currently Amended) The electrostatic discharge protective structure of claim 2, ~~wherein~~where ~~said~~the semiconductor body includes charge carriers of the first conduction type, and at least one well of the second conduction type is embedded in ~~said~~the semiconductor body, and ~~said~~the first and second regions are embedded in ~~said~~the well.

5. (Currently Amended) The electrostatic discharge protective structure of claim 4, ~~wherein~~where ~~said~~the second region laterally encloses ~~said~~the first region.

6. (Currently Amended) The electrostatic discharge protective structure of claim 4, ~~wherein~~where the integrated semiconductor circuit is configured and arranged as a MOS or CMOS circuit.

7. (Currently Amended) The electrostatic discharge protective structure of claim 2, comprising a gate dielectric that spaces ~~said~~the semiconductor body at a distance from the gate electrode.

8. (Currently Amended) The electrostatic discharge protective structure of claim 7, ~~wherein~~where ~~said~~the gate dielectric contains silicon dioxide and ~~said~~the gate electrode contains polysilicon.

9. (Canceled)

10. (Canceled)

11. (Canceled)

12. (Canceled)

13. (Currently Amended) An integrated circuit with electrostatic discharge protection, ~~said~~the integrated circuit comprising:

a circuit to be protected; and

an electrostatic discharge device that is disposed electrically parallel to ~~said~~the circuit to be protected between first and second voltage busses, ~~wherein~~where ~~said~~the electrostatic discharge device includes an electrostatic discharge diode including

(i) a first region doped with a first conduction type material within a substrate;

(ii) a second region doped with a second conduction type material within ~~said~~the substrate; and

(iii) a gate electrode having a width W and located between ~~said~~the first and second regions such that ~~said~~the first and second regions are separated by the width W, where ~~said~~the gate electrode and ~~said~~the second region are both directly connected to the same electrical potential.

14. (Currently Amended) The integrated circuit of claim 13, comprising a gate oxide disposed on

~~said~~the substrate between ~~said~~the first and second conduction regions and underlying ~~said~~the gate electrode.

15. (Currently Amended) The integrated circuit of claim 14, comprising a first electrode disposed on ~~said~~the substrate overlaying ~~said~~the first region, and a second electrode disposed on ~~said~~the substrate overlaying ~~said~~the second region, ~~wherein~~where ~~said~~the first electrode is connected to the first voltage bus and ~~said~~the second electrode is connected to ~~said~~the second bus.

16. (Currently Amended) An integrated circuit with electrostatic discharge protection, ~~said~~the integrated circuit comprising:

a circuit to be protected; and

an electrostatic discharge device that is disposed electrically parallel to ~~said~~the circuit to be protected between first and second voltage busses, ~~wherein~~where ~~said~~the electrostatic discharge device includes an electrostatic discharge diode including

(i) a first doped region doped with a first conduction type material within a substrate;

(ii) a first electrode in communication with ~~said~~the first doped region, ~~said~~the first electrode being coupled to the first voltage bus;

(iii) a second doped region doped with a second conduction type material within ~~said~~the substrate;

(iv) a second electrode in communication with ~~said~~the second doped region, ~~said~~the second electrode being ~~coupled~~ directly connected to the second voltage bus;

(v) an insulator located between ~~said~~the first and second electrodes, and having an insulator dimension that is equal to the distance between ~~said~~the first and second regions;

and

(vi) a gate electrode in communication with and contiguous with ~~said~~the insulator and having a width equal to the width separating the first doped region and the second doped region, where ~~said~~the gate electrode is ~~also~~ directly connected to ~~said~~the second voltage bus.

17. (Currently Amended) The integrated circuit of claim 16, ~~wherein~~where ~~said~~the insulator includes an oxide.

18. (Currently Amended) The integrated circuit of claim 17, ~~wherein~~where ~~said~~the oxide comprises silicon dioxide.

19. (Currently Amended) The integrated circuit of claim 1, ~~wherein~~where ~~said~~the electrostatic discharge diode is laterally formed.

20. (Currently Amended) The integrated circuit of claim 13, ~~wherein~~where ~~said~~the electrostatic discharge diode is laterally formed.

21. (Currently Amended) The integrated circuit of claim 16, ~~wherein~~where ~~said~~the electrostatic discharge diode is laterally formed.

REMARKS

Claims 1-8 and 13-21 have been amended. Claims 1-8 and 13-21 remain for further consideration. No new matter has been added.

The objections and rejections shall be taken up in the order presented in the Official Action.

1-2. Claim 1 currently stands rejected for allegedly being indefinite for a lack of proper antecedent basis.

Claim 1 has been amended to correct the antecedent.

3-4. Claims 1-3, 6-8, 13-15 and 19-20 currently stand rejected for allegedly being anticipated by the subject matter disclosed in U.S. Patent 6,344,385 to Jun et al (hereinafter "Jun").

Claim 1

As amended, claim 1 recites an electrostatic discharge protective device that includes:

> "where the electrostatic discharge protective structure is located between the first and second potential busses and drains off an overvoltage pulse to one of the first and second potential busses, where the electrostatic discharge diode includes a gate electrode located between the first region and the second region, the first region being separated from the second region by a distance that is equal to a width dimension of the gate electrode, and where the gate electrode and the second region are both directly connected to the second supply potential." (emphasis added, cl. 1).

Claim 1 has been amended to now recite that the gate electrode and the second region are both directly connected to the second supply potential.

Upon a fair and proper reading, Jun fails to disclose or suggest a gate electrode and a second region being both directly connected to the second supply potential. As shown in FIG. 3A of Jun, the gate 35 is connected to an RC network, while the p+ implant 36 in Jun is connected to ground.

Thus, Jun clearly discloses that the gate 35 and the p+ implant 36 are not both directly connected to the second supply potential; i.e., ground. As such, Jun fails to anticipate the subject matter of claim 1, since Jun fails to disclose at least the feature of *"where the gate electrode and the second region are both directly connected to the second supply potential."* (cl. 1).

As a result, it is submitted that the anticipation rejection of amended claim 1, together with its dependent claims 2-3, 6-8 and 19, is moot and should be removed, and that amended claim 1, together with claims 2-3, 6-8 and 19, are in condition for allowance and should be passed to issuance.

Claim 13

As amended, claim 13 recites an integrated circuit with electrostatic discharge protection, comprising, *inter alia*, *"(iii) a gate electrode having a width W and located between the first and second regions such that the first and second regions are separated by the width W, where the gate electrode and the second region are both directly connected to the same electrical potential.* (emphasis added).

Claim 13 has been amended to now recite that the gate electrode and the second region are both directly connected to the same electrical potential.

As set forth hereinabove with respect to amended claim 1, Jun neither discloses nor suggests the feature that the gate electrode and the second region are both directly connected to the same electrical potential. Instead, Jun discloses that the gate 35 is connected to an RC circuit, while the p+ region 36 is connected to Ground. Therefore, it is respectfully submitted that Jun is incapable of anticipating the subject matter of amended claim 13.

As a result, it is submitted that the anticipation rejection of amended claim 13 together with

its dependent claims 14-15 and 20, is moot and should be removed, and that amended claim 13, together with claims 14-15 and 20, are in condition for allowance and should be passed to issuance.

5-6. Claim 4 currently stands rejected for allegedly being obvious in view of Jun.

Claim 4 depends indirectly from claim 1, which is patentable for at least the reasons set forth above.

7. Claim 5 currently stands rejected for allegedly being obvious in view of the combined subject matter disclosed in Jun and U.S. Patent 6,060,752 to Williams (hereinafter "Williams").

Claim 5 depends indirectly from claim 1, which is patentable for at least the reasons set forth above.

8. Claims 16-18 and 21 currently stand rejected for allegedly being obvious in view of the combined subject matter disclosed in Jun and U.S. Patent 6,015,993 to Voldman (hereinafter "Voldman").

Claim 16

As amended claim 16 recites an integrated circuit with electrostatic discharge protection, including, *inter alia*:

> "(iv) a second electrode in communication with the second doped region, the second electrode being directly connected to the second voltage bus;
>
> (v) an insulator located between the first and second electrodes, and having an insulator dimension that is equal to the distance between the first and second regions; and
>
> (vi) a gate electrode in communication with and contiguous with the insulator and having a width equal to the width separating the first doped region and the second doped region, where the gate electrode is directly connected to the second voltage bus." (emphasis added, cl. 16)

Claim 16 has been amended to now recite that the second electrode and the gate electrode are both directly connected to the second voltage bus.

Similar to the detailed discussion above with respect to amended claims 1 and 13, Jun neither discloses nor suggests that the second electrode and the gate electrode are both directly connected to the second voltage bus. Instead, Jun discloses that the gate 35 is connected to an RC circuit, while the p+ region 36 is connected to Ground. Accordingly, it is respectfully submitted that Jun is incapable of being combined with Voldman to render obvious amended claim 16.

Further, assuming for the moment that Jun and Voldman are properly combinable, without admitting as much, even if the references were combined as alleged in the Official Action, the resultant combination still fails to disclose the feature of amended claim 16 of both the gate electrode and the second electrode being connected to the second voltage bus.

As a result, it is submitted that the obviousness rejection of amended claim 16, together with its dependent claims 17-18 and 21, is moot and should be removed, and that amended claim 16, together with claims 17-18 and 21, are in condition for allowance and should be passed to issuance.

For all the foregoing reasons, reconsideration and allowance of claims 1-8 and 13-21 is respectfully requested.

If a telephone interview could assist in the prosecution of this application, please call the undersigned attorney.

Respectfully submitted,

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